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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,082	08/19/2003	Sadayoshi Umeda	107337-00050	3060

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EXAMINER	
HOANG, ANN THI	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 06/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/643,082	UMEDA, SADAYOSHI	
	Examiner	Art Unit	
	Ann T. Hoang	2836	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The objection to the disclosure has been withdrawn.

Claim Objections

2. The objection to claim 1 has been withdrawn.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Voldman (US 2002/0097532). Voldman teaches an electrostatic discharge protection circuit 11 for protecting an internal circuit 12 of a semiconductor device 10 against an electrostatic discharge, comprising:

an internal circuit 12 connected with a first and a second power source terminal (14A, 14B);

a transistor 32 switching a source and a drain connected to first and second power source terminals (14A, 14B), respectively; in accordance with a voltage supplied to a back gate 39;

a first diode connected between the first power source terminal 14A and the back gate 39, the first diode supplying a positive discharge voltage generated in the first power source terminal 14A to the back gate 39;

a second diode connected between the second power source terminal 14B and the back gate 39, the second diode supplying a positive discharge voltage generated in the second power source terminal 14B to the back gate 39; and

a voltage-dividing circuit 34 dividing and supplying the discharge voltages to the gate 38 of the transistor 32, the voltage-dividing circuit controlling ON/OFF operation of a source-drain path of the transistor 32.

See Figs. 1 and 4. The ESD protection circuit 11 protects a read head 12 of a disk system 10. Voldman teaches that voltage derived from an ESD event is applied to back gate 39 through diodes shown in Fig. 4, effectively lowering the turn-on voltage of transistor 32. A voltage-dividing circuit 34 is one of many implementations that may be used to apply a voltage to the gate 38 of transistor 32. See paragraphs 5, 18 and 20.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Voldman (US 2002/0097532). In the reference, transistor 32 is shown to be an NMOS transistor in Fig. 4. Based on the known operation of NMOS transistors, it is understood that transistor 32 comprises:

a first power source terminal side serving as a drain when the positive discharge voltage is supplied from the first power source terminal 1A to the back gate 39, and

a second power source terminal side serving as a drain when the positive discharge voltage is supplied from the second power source terminal 14B to the back gate 39.

Note that replacement of the NMOS transistor 32 with a PMOS transistor would result in an opposite outcome, wherein the first power source terminal side would as a source when the positive discharge voltage was supplied from the first power source terminal 1A to the back gate 39, and the second power source terminal side would serve as a source when the positive discharge voltage was supplied from the second power source terminal 14B to the back gate 39. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a PMOS transistor instead of an NMOS transistor because it would be functionally equivalent in the ESD protection circuit.

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Voldman (US 2002/0097532), as applied to claim 1 above, and further in view of Krzentz (US 5,796,296). Voldman does not teach that voltage-dividing circuit 34 equally divides the discharge voltage before supplying the voltage to gate 38.

However, Krzentz teaches a two-to-one voltage-dividing circuit wherein the output voltage is one half of the input voltage. See all figures and column 2, lines 22-37. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the two-to-one voltage divider of Krzentz in the electrostatic discharge protection circuit of Voldman in order to equally divide the discharge voltage. Equal voltage division would serve as a control method to keep the gate of the transistor indiscriminate between a discharge voltage supplied by the first power source terminal and that supplied by the second power source terminal, therefore allowing consistent operation of the transistor even as the source and drain were switched.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Voldman (US 2002/0097532), as applied to claim 1 above, and further in view of Zhou (US 5,446,644). Voldman does not teach that voltage-dividing circuit 34 unidirectionally runs a current caused by the discharge voltage.

However, Zhou discloses a voltage-dividing circuit for unidirectional transmission that divides a high voltage input into a low voltage DC output (see Fig. 1 and abstract). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the unidirectional voltage-dividing circuit of Zhou in the electrostatic discharge protection circuit of Voldman in order to divide a high discharge voltage input into a low voltage output for the gate of the transistor.

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Voldman (US 2002/0097532), as applied to claim 1 above, and further in view of the acknowledged prior art of Applicant's disclosure. Voldman does not teach diodes

connected between an input/output terminal of internal circuit 12 and first and second power source terminals (14A, 14B), respectively.

However, the acknowledged prior art discloses diodes (D7, D8) connected between an input/output terminal V of an internal circuit 30 and first and second power source terminals (VD, VS), respectively, the diodes (D7, D8) carrying the discharge voltage produced in input/output terminal V to first and second power source terminals (VD, VS), respectively, in the form of an electric current. It would have been obvious to one of ordinary skill in the art at the time of the invention to include the diodes of the acknowledged prior art in the electrostatic discharge protection circuit of Voldman in order to disperse discharge voltages produced in any input/output terminal of additional internal circuits connected between the first and second power source terminals.

Response to Arguments

Applicant's arguments with respect to claims 1-5 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ann T. Hoang, whose telephone number is 571-272-2724. The examiner can normally be reached Mondays through Fridays, 8:00 a.m. to 5:00 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus, can be reached at 571-272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ATH
31 May 2006

Stephen W. Jackson
6-8-06

STEPHEN W. JACKSON
PRIMARY EXAMINER